Claims

[c1] 1. A semiconductor device, comprising:
a capacitor, a calibration resistor, and a calibration circuit formed within the semiconductor device, wherein a voltage (Vin) applied to the calibration resistor is adapted to produce a current flow through the calibration resistor to charge the capacitor, wherein the calibration circuit is adapted to measure an actual time (t_{actual}) required to charge the capacitor, and wherein the calibration circuit is further adapted calculate an actual resistance value (R_{actual}) of the calibration resistor based on t_{actual} and a capacitance value (C) of the capacitor.

[c2] 2. The semiconductor device of claim 1, wherein the calibration circuit is further adapted to calculate an expected time ($t_{expected}$) to charge the capacitor based on an expected resistance value ($R_{expected}$) of the calibration resistor and C.

[c3] 3. The semiconductor device of claim 2, wherein the calibration circuit is further adapted to determine a time differential (Δt) between t_{actual} and $t_{expected}$, and wherein Δt is adapted to determine a percentage of deviation of resistance R_{actual} from $R_{expected}$ of the calibration resistor.

[c4] 4. The semiconductor device of claim 3, wherein the semiconductor device further comprises a plurality of resistors, and wherein each of the plurality of resistors comprises a percentage of deviation of resistance of an actual resistance from an expected resistance that is about equal to the percentage of deviation of resistance R_{actual} from $R_{expected}$ of the calibration resistor.

[c5] 5. The semiconductor device of claim 4, wherein Δt is further adapted to determine a change of resistance value for each of the plurality of resistors.

[c6] 6. The semiconductor device of claim 5, wherein each of the plurality of resistors comprises a resistance value that is not equal to a resistance value of the calibration resistor.

[c7] 7. The semiconductor device of claim 5, wherein the calibration resistor is adapted to be permanently removed from the semiconductor device after Δt determines the change of resistance value for each of the plurality of resistors.

[c8] 8. The semiconductor device of claim 5, wherein the semiconductor device further comprises a bank of resistors, and wherein each of the bank of resistors is adapted to be connected in series or in parallel with each

of the plurality of resistors such that a resistance value of a combination of a first resistor of the plurality of resistors and at least one resistor of the bank of resistors equals an expected resistance value of the first resistor.

[c9] 9. The semiconductor device of claim 5, wherein the calibration circuit is adapted to continuously determine Δt, wherein Δt continuously determines a change of resistance value for the calibration resistor, and wherein Δt continuously determines the change of resistance value for each of the plurality of resistors.

[c10] 10. The semiconductor device of claim 9, wherein the semiconductor device further comprises a bank of resistors, wherein each of the bank of resistors is adapted to be connected in series or in parallel with each of the plurality of resistors such that a resistance value of a combination of a first resistor of the plurality of resistors and at least one resistor of the bank of resistors equals an expected resistance value of the first resistor, and wherein each of the bank of resistors is further adapted to be connected in series or in parallel with the calibration resistor such that a resistance value of a combination of the calibration and at least one resistor of the bank of resistors equals $R_{expected}$ of the calibration resistor.

[c11] 11. A calibration method, comprising:
providing a capacitor, a calibration resistor, and a calibration circuit formed within a semiconductor device;
providing a current flow through the calibration resistor to charge the capacitor;
measuring by the calibration circuit, an actual time (t_{actual}) required to charge the capacitor; and
determining by the calibration circuit, an actual resistance value (R_{actual}) of the calibration resistor based on t_{actual} and a capacitance value (C) of the capacitor.

[c12] 12. The method of claim 11, further comprising calculating by the calibration circuit an expected time ($t_{expected}$) to charge the capacitor based on an expected resistance value ($R_{expected}$) of the calibration resistor and C.

[c13] 13. The method of claim 12, further comprising determining by the calibration circuit, a time differential (Δt) between t_{actual} and $t_{expected}$, and
determining from Δt, a percentage of deviation of resistance R_{actual} from $R_{expected}$ of the calibration resistor.

[c14] 14. The method of claim 13, further comprising providing a plurality of resistors within the semiconductor device, wherein each of the plurality of resistors comprises a percentage of deviation of resistance of an actual resistance from an expected resistance that is about equal

to the percentage of deviation of resistance R_{actual} from $R_{expected}$ of the calibration resistor.

[c15] 15. The method of claim 14, further comprising determining from Δt, a change of resistance value for each of the plurality of resistors.

[c16] 16. The method of claim 15, wherein each of the plurality of resistors comprises a resistance value that is not equala resistance value of the calibration resistor.

[c17] 17. The method of claim 15, further comprising permanently removing the calibration resistor from the semiconductor device after determining from Δt the change of resistance value for each of the plurality of resistors.

[c18] 18. The semiconductor device of claim 15, further comprising a bank of resistors within the semiconductor device; and
connecting at least one resistor from the bank of resistors in series or in parallel with at least one of the plurality of resistors such that a resistance value of a combination of a first resistor of the plurality of resistors and at least one resistor of the bank of resistors equals an expected resistance value of the first resistor.

[c19] 19. The method of claim 15, further comprising continuously determining by the calibration circuit, Δt;

continuously determining from Δt, a change of resistance value for the calibration resistor; and
continuously determining from Δt, the change of resistance value for each of the plurality of resistors.

[c20] 20. The method of claim 19, further comprises a bank of resistors within the semiconductor device;
connecting at least one resistor from the bank of resistors in series or in parallel with at least one of the plurality of resistors such that a resistance value of a combination of a first resistor of the plurality of resistors and at least one resistor of the bank of resistors equals an expected resistance value of the first resistor.; and
connecting at least one resistor from the bank of resistors in series or in parallel with the calibration resistor such that a resistance value of a combination of the calibration and at least one resistor of the bank of resistors equals $R_{expected}$ of the calibration resistor.